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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,688	03/03/2004	Nimrod Agmon	MP0404	2295

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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/790,688	AGMON, NIMROD	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004-13 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is with regards to Application 10/790,688 filed 03 March 2004, and amended 13 August 2004. Claims 1 – 14 are pending in this Application.

Claim Objections

2. Claims 5, 11, 13 and 14 are objected to because of the following informalities:

- Claims 5 and 11, line 2, delete "a state" and insert --the state--.
- Claims 13 and 14 delete "verified" and insert --tested--.
- In claims 13 and 14, Applicant did not specify what type of semiconductor is being tested. Is it a semiconductor circuit, semiconductor wafer, semiconductor device?

3. Appropriate correction is required.

Double Patenting

4. Claims 1, 4, 5, 7, 10, 11, 13 and 14 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 5, 6, 8, 12, 13, 15 and 16, respectively, of copending Application No. 10/806,481. Although the conflicting claims are not identical, they are not patentably distinct from each other because "a method and program for testing a design of a circuit" in the instant Application (independent claims 1 and 7) are similar to "a method and program for verifying a design of the circuit" in the copending Application (independent claims 1 and 8).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1 – 6 and 7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not refer to, or describe, the claimed limitation of ***"testing*** a design", but teaches instead "***verifying*** a design". The Examiner will assume that 'testing" and "verifying" are identical.

7. Claims 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not refer to, or describe, "the ***semiconductor*** verified by the method, or program", as claimed.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 7 – 12 and 14 are rejected under 35 U.S.C. 101 because these claims refer only to "a ***computer program*** for testing" (i.e., does not include a new and useful process, machine, manufacture or composition of matter).

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1 – 14 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,944,838 B2 to McMillan.

11. Referring to claims 1 and 7, McMillan cites a method (claim 1) and a computer program (claim 7 – see also col. 9, ll. 12 – 25) for verifying (i.e., testing) a design of a circuit (see Abstract; col. 1, ll. 13 – 18), comprising: (a) providing a model of the design (see col. 1, ll. 45 – 48); (b) providing a first property for the design, wherein the first property describes a first behavior (see Fig. 1, block 120; Fig. 2, block 210; col. 2, line 29 – col. 3, line 13); (c) checking the model using the first property and an environment of the design at a reset state until an example of the first behavior occurs (see again Figs. 1 and 2; col. 1, line 29 – col. 3, line 13); and (d) providing a second property for the design wherein the second property describes a second behavior, and checking the model using the second property and an environment of the design at a state when the

example of the first behavior occurs (these elements are clearly cited in Figs. 1 and 2; col. 2, line 29 – col. 5, line 48). Thus, McMillan clearly discloses, or at the very least suggests, all the claimed limitations.

12. As per claims 2 and 3, see Fig. 2, block 210; col. 2, line 64 – col. 3, line 23, which disclose, or at the very least suggest, the claimed limitations pertaining to the use of Boolean expressions for describing the first property and for checking the model.

13. Regarding claims 4 and 5, see Fig. 1, block 110; Fig. 2, block 232; col. 2, ll. 29 – 37; col. 3, ll. 2 – 13, which teach the claimed elements pertaining to providing the environment (i.e., design description) at the reset state (claim 4) and at a state when an example of the first behavior occurs (claim 5).

14. As to claim 6, see (13) above, as well as col. 2, line 64 – col. 3, line 33, which teach the limitations for providing the environment of the design at the state when an example of the first behavior occurs, as claimed.

15. Claims 8 – 12 contain the same limitations found in claims 2 – 6, respectively, and thus the same rejections also apply.

16. Pursuant to claims 13 and 14, see col. 8, line 63 – col. 9, line 11, which teach the claimed element of semiconductor devices.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 7,020,856 B2 to Singhal et al. discloses a methodology for verifying properties of a circuit model in context of given environmental constraints, whereas

verification of a specified property is performed by analyzing only a portion of the circuit model.

U.S. Patent No. 6,560,758 B1 to Jain cites a system and method for representing digital circuits and systems in multiple partitions of Boolean space, and for performing circuit and system validation using multiple partitions.

U.S. Patent No. 6,698,003 B2 to Baumgartner et al. teaches a design verification system comprising a set of modular verification engines.

U.S. Patent No. 6,816,827 B1 recites a design verification method for verifying hardware designs utilizing combinational loop logic.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
12 April 2006

PAUL DINH
PRIMARY EXAMINER